REMARKS

Claims 1-24 are pending in the application. Claim 17 is objected to. Claims 1-24 are rejected under 35 U.S.C. §102(e). Applicants address these objections and rejections below.

Applicants amended claim 17 to more clearly state the claimed subject matter. Hence, no prosecution history estoppel arises from the amendment to claim 17. *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 62 U.S.P.Q.2d 1705, 1711-12 (2002); 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2000). Further, the amendment made to claim 17 was not made for a substantial reason related to patentability and therefore no prosecution history estoppel arises from such an amendment. *See Festo Corp.*, 62 U.S.P.Q.2d 1705 at 1707 (2002); *Warner-Jenkinson Co. v. Hilton Davis Chemical Co.*, 41 U.S.P.Q.2d 1865, 1873 (1997).

I. OBJECTIONS TO THE CLAIMS:

The Examiner has objected to the phrase "said method" in claim 17 when the claim preamble recites "a photolithography processing system." Office Action (6/13/2006), page 2. Applicants amended claim 17 to more clearly state the claimed subject matter and removed the "said" in front of "method" thereby eliminating antecedent basis problems. Accordingly, Applicants respectfully request the Examiner to withdraw the objection to claim 17.

II. REJECTIONS UNDER 35 U.S.C. §102(e):

The Examiner has rejected claims 1-24 under 35 U.S.C. §102(e) as being anticipated by Maurer et al. (U.S. Publication No. 2004/0063000) (hereinafter "Maurer"). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

Applicants respectfully assert that Maurer does not disclose "evaluating manufacturability of structures within each simulation" as recited in claim 1. The Examiner cites paragraphs [0045]0046] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 3. Applicants respectfully traverse and assert that Maurer instead discloses that because of integrated circuit complexity, computer-based integrated circuit design and verification tools can be used to determine the masks and mask patterns necessary to realize a selected integrated circuit design. [0045]. Maurer further discloses that such computer-based tools can be configured to define mask patterns based on one or more resolution enhancement techniques (RETs). [0046]. Maurer additionally discloses that a computer-based design tool can be configured to access layout data stored in a database and apply or select one or more RETs based on a consideration of one or more selected features or a consideration of all or substantially all features. [0046]. Maurer further discloses that because a computer-based tool can access a stored layout or generate a layout based on a circuit design, a number of lithographic processes can be evaluated. [0046]. Hence, Maurer discloses the use of using computer-based tools to determine the masks and mask patterns necessary to realize a selected integrated circuit design using one or more resolution enhancement techniques. Maurer further discloses evaluating lithographic processes. However, there is no language in the cited passages that discloses evaluating manufacturability of structures. Neither is there any language in the cited passages that discloses evaluating manufacturability of structures within each simulation. Thus, Maurer does not disclose all of the limitations of claim 1, and thus Maurer does not anticipate claim 1. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "selecting one or more RETs that provide optimal manufacturability" as recited in claim 1. The Examiner cites paragraphs [0046]; [0050]; and [0062] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), pages 3-4. Applicants respectfully traverse.

Maurer instead discloses that a computer-based design tool can be configured to access layout data stored in a database and apply or select one or more RETs based

on a consideration of one or more selected features or a consideration of all or substantially all features. [0046]. Maurer further discloses that because a computer-based tool can access a stored layout or generate a layout based on a circuit design, a number of lithographic processes can be evaluated. [0046]. Maurer additionally discloses that because a computer-based tool can access a stored layout or generate a layout based on a circuit design, a number of lithographic processes can be evaluated. [0046]. In addition, Maurer discloses that DDL and other off-axis illumination RETs are generally optimized for a particular pitch, typically a rather dense pitch. [0050]. Furthermore, Maurer discloses that using the MEF curve 502, features sizes in a particular design can be identified as small, intermediate, or large based on the sign of the MEF and an appropriate technique used to define corresponding portions of a mask. [0060]. Hence, Maurer discloses the use of using computer-based tools to determine the masks and mask patterns necessary to realize a selected integrated circuit design using one or more resolution enhancement techniques. Maurer further discloses identifying feature sizes in a design as small, intermediate, or large based on the sign of the MEF. There is no language in the cited passages that discloses selecting one or more RETs that provide optimal manufacturability. Thus, Maurer does not disclose all of the limitations of claim 1, and thus Maurer does not anticipate claim 1. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "in a photolithography processing system having an associated numerical aperture (NA) value in which a reticle having a set of reticle parameters is exposed to an illuminator having a set of illuminator parameters to pattern a wafer with a desired layout" as recited in claim 17. The Examiner cites paragraphs [0080-0081] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 4. Applicants respectfully traverse and assert that Maurer instead discloses that various process tools can be remotely located from the client computer 1102. [0080]. Maurer further discloses that the term 'twin' phase edges generally refers to phase edges that are placed so that images of the phase edges merge or partially merge. [0081]. There is no language in the cited passages that disclose a photolithography system having an associated numerical aperture. Neither is there any language in the cited passages that discloses

a photolithography system having an associated numerical aperture in which a reticle having a set of reticle parameters is exposed to an illuminator. Neither is there any language in the cited passages that discloses a photolithography system having an associated numerical aperture in which a reticle having a set of reticle parameters is exposed to an illuminator having a set of illuminator parameters to pattern a wafer with a desired layout. Thus, Maurer does not disclose all of the limitations of claim 17, and thus Maurer does not anticipate claim 17. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "simulating how the desired layout will pattern on a wafer for a plurality of combinations of different NA values, illuminator parameters and reticle parameters" as recited in claim 17. The Examiner cites paragraphs [0003]; [0022]; [0031]; [0032]; [0044]; [0046]; [0049]; [0050]; [0060]; [0062]; and [0063] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 4. Applicants respectfully traverse.

Maurer instead discloses that a computer-based design tool can be configured to access layout data stored in a database and apply or select one or more RETs based on a consideration of one or more selected features or a consideration of all or substantially all features. [0046]. Maurer further discloses that because a computer-based tool can access a stored layout or generate a layout based on a circuit design, a number of lithographic processes can be evaluated. [0046]. Maurer additionally discloses that because a computer-based tool can access a stored layout or generate a layout based on a circuit design, a number of lithographic processes can be evaluated. [0046]. In addition, Maurer discloses that DDL and other off-axis illumination RETs are generally optimized for a particular pitch, typically a rather dense pitch. [0050]. Furthermore, Maurer discloses that using the MEF curve 502, features sizes in a particular design can be identified as small, intermediate, or large based on the sign of the MEF and an appropriate technique used to define corresponding portions of a mask. [0060]. Hence, Maurer discloses the use of using computer-based tools to determine the masks and mask patterns necessary to realize a selected integrated circuit design using one or more resolution enhancement techniques. Maurer further discloses identifying feature sizes in a design as small, intermediate, or large based on

the sign of the MEF. There is no language in the cited passages that discloses simulating how the desired layout will pattern on a wafer for a plurality of combinations of different NA values, illuminator parameters and reticle parameters. Thus, Maurer does not disclose all of the limitations of claim 17, and thus Maurer does not anticipate claim 17. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "for each combination of NA values, illuminator parameters and reticle parameters, classifying structures within the associated simulated layouts based on manufacturability" as recited in claim 17. The Examiner cites paragraphs [0063-0064] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 5. Applicants respectfully traverse and assert that Maurer instead discloses that small features can be identified approximately as features for which a minimum aerial image intensity decreases with increases in feature sizes. [0063]. Maurer further discloses that layout processing using feature size identification. [0064]. There is no language in the cited passages that discloses classifying structures within the associated simulated layouts based on manufacturability. Neither is there any language in the cited passages that discloses classifying structures within the associated simulated layouts based on manufacturability for each combination of NA values, illuminator parameters and reticle parameters. Thus, Maurer does not disclose all of the limitations of claim 17, and thus Maurer does not anticipate claim 17. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "selecting at least one combination of NA value, illuminator parameters and reticle parameters based on the classifying step" as recited in claim 17. The Examiner cites paragraphs [0046]; [0050]; and [0062] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 5. Applicants respectfully traverse and assert that Maurer instead discloses that a computer-based design tool can be configured to access layout data stored in a database and apply or select one or more RETs based on a consideration of one or more selected features or a consideration of all or substantially all features. [0046]. Maurer further discloses that because a computer-based tool can access a stored layout or generate a layout based on a circuit design, a

number of lithographic processes can be evaluated. [0046]. Maurer additionally discloses that because a computer-based tool can access a stored layout or generate a layout based on a circuit design, a number of lithographic processes can be evaluated. [0046]. In addition, Maurer discloses that DDL and other off-axis illumination RETs are generally optimized for a particular pitch, typically a rather dense pitch. [0050]. Maurer additionally discloses that groupings of pattern features into so-called small, intermediate, and large pattern feature groups can be arranged based directly on feature size. [0062]. Hence, Maurer discloses the use of using computer-based tools to determine the masks and mask patterns necessary to realize a selected integrated circuit design using one or more resolution enhancement techniques. Maurer further discloses that the groupings of pattern features into small, intermediate, and large pattern feature groups can be arranged based directly on feature size. There is no language in the cited passages that discloses selecting at least one combination of NA value, illuminator parameters and reticle parameters. Neither is there any language in the cited passages that discloses selecting at least one combination of NA value, illuminator parameters and reticle parameters based on the classifying step. Thus, Maurer does not disclose all of the limitations of claim 17, and thus Maurer does not anticipate claim 17. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "simulating how the desired layout will print on the wafer for a plurality of RET process windows, each RET process window corresponding to a plurality of lithography process parameters" as recited in claim 22. The Examiner cites paragraphs [0031]; [0044]; [0046]; [0059]; [0060] and [0062] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 5. Applicants respectfully traverse.

Maurer instead discloses that a computer-based design tool can be configured to access layout data stored in a database and apply or select one or more RETs based on a consideration of one or more selected features or a consideration of all or substantially all features. [0046]. Maurer further discloses that because a computer-based tool can access a stored layout or generate a layout based on a circuit design, a number of lithographic processes can be evaluated. [0046]. Maurer additionally

discloses that because a computer-based tool can access a stored layout or generate a layout based on a circuit design, a number of lithographic processes can be evaluated. [0046]. In addition, Maurer discloses that DDL and other off-axis illumination RETs are generally optimized for a particular pitch, typically a rather dense pitch. [0050]. Furthermore, Maurer discloses that using the MEF curve 502, features sizes in a particular design can be identified as small, intermediate, or large based on the sign of the MEF and an appropriate technique used to define corresponding portions of a mask. [0060]. Hence, Maurer discloses the use of using computer-based tools to determine the masks and mask patterns necessary to realize a selected integrated circuit design using one or more resolution enhancement techniques. Maurer further discloses identifying feature sizes in a design as small, intermediate, or large based on the sign of the MEF.

There is no language in the cited passages that discloses simulating how the desired layout will print on the wafer for a plurality of RET process windows. Neither is there any language in the cited passages that discloses simulating how the desired layout will print on the wafer for a plurality of RET process windows, each RET process window corresponding to a plurality of lithography process parameters. Thus, Maurer does not disclose all of the limitations of claim 22, and thus Maurer does not anticipate claim 22. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "for each RET process window, classifying edges of structures within the simulated layout based on manufacturability" as recited in claim 22. The Examiner cites paragraphs [0062-0064] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 5. Applicants respectfully traverse and assert that Maurer instead discloses that groupings of pattern features into so-called small, intermediate, and large pattern feature groups can be arranged based directly on feature size. [0062]. Maurer further discloses that small features can be identified approximately as features for which a minimum aerial image intensity decreases with increases in feature sizes. [0063]. Maurer further discloses that layout processing using feature size identification. [0064]. There is no language in the cited passages that discloses

classifying edges of structures within the simulated layout. Neither is there any language in the cited passages that discloses classifying edges of structures within the simulated layout based on manufacturability. Neither is there any language in the cited passages that discloses classifying edges of structures within the simulated layout based on manufacturability for each RET process window. Thus, Maurer does not disclose all of the limitations of claim 22, and thus Maurer does not anticipate claim 22. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "selecting one or more RET process windows that provide optimal manufacturability" as recited in claim 22. The Examiner cites paragraphs [0046]; [0050]; and [0062] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 5. Applicants respectfully traverse.

Maurer instead discloses that a computer-based design tool can be configured to access layout data stored in a database and apply or select one or more RETs based on a consideration of one or more selected features or a consideration of all or substantially all features. [0046]. Maurer further discloses that because a computer-based tool can access a stored layout or generate a layout based on a circuit design, a number of lithographic processes can be evaluated. [0046]. Maurer additionally discloses that because a computer-based tool can access a stored layout or generate a layout based on a circuit design, a number of lithographic processes can be evaluated. [0046]. In addition, Maurer discloses that DDL and other off-axis illumination RETs are generally optimized for a particular pitch, typically a rather dense pitch. [0050]. Furthermore, Maurer discloses that groupings of pattern features into so-called small, intermediate, and large pattern feature groups can be arranged based directly on feature size. [0062]. Hence, Maurer discloses the use of using computer-based tools to determine the masks and mask patterns necessary to realize a selected integrated circuit design using one or more resolution enhancement techniques. Maurer further discloses that groupings of pattern features can be arranged into small, intermediate, and large pattern feature groups based directly on feature size. There is no language in the cited passages that discloses selecting one or more RET process windows.

Neither is there any language in the cited passages that discloses selecting one or more RET process windows that provide optimal manufacturability. Thus, Maurer does not disclose all of the limitations of claim 22, and thus Maurer does not anticipate claim 22. M.P.E.P. §2131.

Claims 2-16 each recite combinations of features of independent claim 1, and hence claims 2-16 are not anticipated by Maurer for at least the reasons that claim 1 is not anticipated by Maurer.

Claims 18-21 each recite combinations of features of independent claim 17, and hence claims 18-21 are not anticipated by Maurer for at least the reasons that claim 17 is not anticipated by Maurer.

Claims 23-24 each recite combinations of features of independent claim 22, and hence claims 23-24 are not anticipated by Maurer for at least the reasons that claim 22 is not anticipated by Maurer.

Claims 2-16, 18-21 and 23-24 recite additional features, which, in combination with the features of the claims upon which they depend, are not anticipated by Maurer.

For example, Maurer does not disclose "performing optical rule checking (ORC) on structures within each simulation; and for each simulation, calculating a percentage of optically different edges that demonstrate acceptable manufacturability" as recited in claim 2 and similarly in claims 18 and 24. The Examiner cites paragraphs [0072] and [0075] of Maurer as disclosing the above-cited claim limitations. Office Action (6/13/2006), page 5. Applicants respectfully traverse and assert that Maurer instead discloses that the hierarchical database 702 is configured for access by layout verification tools such as a layout versus schematic (LVS) tool 708, a design rule check (DRC) tool 710, an optical rule checking (ORC) tool 712, a phase-shift mask (PSM) tool 714, and an optical process correction (OPC) tool 716 that are configured to verify that transformation to a physical layout has not introduced errors, and that the final layout is in compliance with appropriate

geometric design rules or other design rules. [0072]. Maurer further discloses that the tool 700 also includes a data export component 718 configured to provide data to a circuit manufacturing process 720. [0075]. There is no language in the cited passages that discloses that for each simulation, calculating a percentage of optically different edges. Neither is there any language in the cited passages that discloses that for each simulation, calculating a percentage of optically different edges that demonstrate acceptable manufacturability. Thus, Maurer does not disclose all of the limitations of claims 2, 18 and 24, and thus Maurer does not anticipate claims 2, 18 and 24. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "selecting RETs that correspond to simulations having a percentage of acceptable optically different edges that is greater than a predefined value" as recited in claim 3. The Examiner cites paragraphs [0072] and [0075] of Maurer as disclosing the above-cited claim limitations. Office Action (6/13/2006), page 5. Applicants respectfully traverse and assert that Maurer instead discloses that the hierarchical database 702 is configured for access by layout verification tools such as a layout versus schematic (LVS) tool 708, a design rule check (DRC) tool 710, an optical rule checking (ORC) tool 712, a phase-shift mask (PSM) tool 714, and an optical process correction (OPC) tool 716 that are configured to verify that transformation to a physical layout has not introduced errors, and that the final layout is in compliance with appropriate geometric design rules or other design rules. [0072]. Maurer further discloses that the tool 700 also includes a data export component 718 configured to provide data to a circuit manufacturing process 720. [0075]. There is no language in the cited passages that discloses selecting RETs. Neither is there any language in the cited passages that discloses selecting RETs that correspond to simulations. Neither is there any language in the cited passages that discloses selecting RETs that correspond to simulations having a percentage of acceptable optically different edges that is greater than a predefined value. Thus, Maurer does not disclose all of the limitations of claim 3, and thus Maurer does not anticipate claim 3. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "wherein each RET includes a combination of illuminator parameters, numerical aperture (NA) and mask parameters" as recited in claim 4. The Examiner cites paragraphs [0003]; [0049] and [0050] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 6. Applicants respectfully traverse and assert that Maurer instead discloses that the basic resolution of an optical lithography system is generated related to a ratio of Lambda/NA of an optical wavelength of the radiation used for exposure to the numerical aperture of the optical system used to direct radiation from an irradiated mask to the wafer. [0003]. Maurer further discloses that other RETs such as double-exposure dipole lithography (DDL) use off-axis mask illumination. [0049]. Maurer further discloses that the DDL and other off-axis illumination RETs are generally optimized for a particular pitch, typically a rather dense pitch. [0050]. There is no language in the cited passages that discloses that each RET includes a combination of illuminator parameters, numerical aperture (NA) and mask parameters. Thus, Maurer does not disclose all of the limitations of claim 4, and thus Maurer does not anticipate claim 4. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "wherein the illuminator parameters include at least one of (i) illuminator source shape, (ii) number of poles, (iii) orientation of poles, (iv) inner radius, (v) outer radius, and (vi) wedge angle" as recited in claim 5 and similarly in claim 20. The Examiner cites paragraph [0049] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 6. Applicants respectfully traverse and assert that Maurer instead discloses that other RETs such as double-exposure dipole lithography (DDL) use off-axis mask illumination. [0049]. There is no language in the cited passage that discloses that the illuminator parameters include at least one of (i) illuminator source shape, (ii) number of poles, (iii) orientation of poles, (iv) inner radius, (v) outer radius, and (vi) wedge angle. Thus, Maurer does not disclose all of the limitations of claims 5 and 20, and thus Maurer does not anticipate claims 5 and 20. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "wherein the mask parameters include at least one of mask type and mask transmission" as recited in claim 6. The Examiner cites paragraphs [0003]; [0049] and [0050] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 6. Applicants respectfully traverse. As stated above, Maurer instead discloses that the basic resolution of an optical lithography system is generated related to a ratio of Lambda/NA of an optical wavelength of the radiation used for exposure to the numerical aperture of the optical system used to direct radiation from an irradiated mask to the wafer. [0003]. Maurer further discloses that other RETs such as double-exposure dipole lithography (DDL) use off-axis mask illumination. [0049]. Maurer further discloses that the DDL and other off-axis illumination RETs are generally optimized for a particular pitch, typically a rather dense pitch. [0050]. There is no language in the cited passages that discloses that mask parameters include at least one of mask type and mask transmission. Thus, Maurer does not disclose all of the limitations of claim 6, and thus Maurer does not anticipate claim 6. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "wherein the simulating step includes simulating variations over a predetermined range in at least one of focus, exposure and the mask" as recited in claim 7 and similarly in claim 23. The Examiner cites paragraph [0032] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 6. Applicants respectfully traverse and assert that Maurer instead discloses that Figure 5A shows mask error function (MEF) and critical dimension on a wafer as a function of critical dimension on a mask obtained by simulations based on chromeless-phase lithography (CPL) using an exposure wavelength of 193 nm and an optical system numeral aperture of 0.75. [0032]. There is no language in the cited passage that discloses that the simulating step includes simulating variations over a predetermined range. Neither is there any language in the cited passage that discloses that the simulating step includes simulating variations over a predetermined range in at least one of focus, exposure and the mask. Thus, Maurer does not disclose all of the limitations of claims 7 and 23, and thus Maurer does not anticipate claims 7 and 23. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "wherein performing ORC includes checking structures within the simulations based on one of aerial image metrics, resist image metrics, and post exposure bake metrics" as recited in claim 8 and similarly in claim 19. The Examiner cites paragraphs [0020] and [0056] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 6. Applicants respectfully traverse and assert that Maurer does not disclose that Figures 1A-1B are graphs of simulated normalized image log slopes (NILS) as a function of defocus for lithographic exposures using alternating phase-shift masks, double-exposure dipole lithography, and chromeless phase lithography for pattern regions having isolated lines and nested lines. [0020]. Maurer further discloses that Figures 4A-4B are plan views of simulated DDL exposures with and without, respectively, OPC. [0056]. There is no language in the cited passages that discloses performing ORC. Neither is there any language in the cited passages that discloses that performing ORC includes checking structures within the simulations. Neither is there any language in the cited passages that discloses that performing ORC includes checking structures within the simulations based on one of aerial image metrics, resist image metrics, and post exposure bake metrics. Thus, Maurer does not disclose all of the limitations of claims 8 and 19, and thus Maurer does not anticipate claims 8 and 19. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "wherein the aerial image metrics include at least one of image edge slope, image edge log slope, contrast, minimum intensity, maximum intensity, edge placement error and intensity at a given distance" as recited in claim 9. The Examiner cites paragraphs [0052-0054]; and [0059] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 6. Applicants respectfully traverse and assert that Maurer instead discloses that Figures 1A-1B are graphs of normalized image log slopes (NILS) as a function of defocus that illustrate the performance of alt-PSM, DDL, and CPL for an isolated 65 nm wide line. [0052]. Maurer further discloses that Figures 2A-2D illustrate simulated aerial image intensities obtained by simulated exposure of a wide (310 nm) phase region and a narrow (70 nm) phase region using CPL. [0053]. Maurer additionally discloses that although CPL exhibits some limitations in pattern-

transfer of phase regions such as the phase region 200, such pattern transfer can be substantially improved using OPC. [0054]. Furthermore, Maurer discloses that corrections can be applied by inversion of the process model and/or by iterative changes of geometry data that define the masks in order to generate a printed image as close as possible to an intended image. [0059]. There is no language in the cited passages that discloses that the aerial image metrics include at least one of image edge slope, image edge log slope, contrast, minimum intensity, maximum intensity, edge placement error and intensity at a given distance. Thus, Maurer does not disclose all of the limitations of claim 9, and thus Maurer does not anticipate claim 9. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "recording values for at least one of the metrics in a searchable data table structure" as recited in claim 10. The Examiner cites paragraphs [0052-0054]; and [0059] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 6. Applicants respectfully traverse. As stated above, Maurer instead discloses that Figures 1A-1B are graphs of normalized image log slopes (NILS) as a function of defocus that illustrate the performance of alt-PSM, DDL, and CPL for an isolated 65 nm wide line. [0052]. Maurer further discloses that Figures 2A-2D illustrate simulated aerial image intensities obtained by simulated exposure of a wide (310 nm) phase region and a narrow (70 nm) phase region using CPL. [0053]. Maurer additionally discloses that although CPL exhibits some limitations in pattern-transfer of phase regions such as the phase region 200, such pattern transfer can be substantially improved using OPC. [0054]. Furthermore, Maurer discloses that corrections can be applied by inversion of the process model and/or by iterative changes of geometry data that define the masks in order to generate a printed image as close as possible to an intended image. [0059]. There is no language in the cited passages that discloses recording values for at least one of the metrics in a searchable data table structure. Thus, Maurer does not disclose all of the limitations of claim 10, and thus Maurer does not anticipate claim 10. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "based on the simulating step, providing a graphical representation indicating the manufacturability of the layout for the plurality of RETs" as recited in claim 11. The Examiner cites paragraphs [0071-0072] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 6. Applicants respectfully traverse and assert that Maurer instead discloses that the layout data portion of Figure 7D includes a top level cell 750 that includes second level cells 752, 753, 754 and a layout feature 756. [0071]. Maurer further discloses that the hierarchical database 702 is configured for access by layout verification tools such as a layout versus schematic (LVS) tool 708, a design rule check (DRC) tool 710, an optical rule checking (ORC) tool 712, a phase-shift mask (PSM) tool 714, and an optical process correction (OPC) tool 716 that are configured to verify that transformation to a physical layout has not introduced errors, and that the final layout is in compliance with appropriate geometric design rules or other design rules. [0072]. There is no language in the cited passages that discloses that based on the simulating step, providing a graphical representation indicating the manufacturability of the layout for the plurality of RETs. Thus, Maurer does not disclose all of the limitations of claim 11, and thus Maurer does not anticipate claim 11. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "exposing a wafer to an illumination source having selected illuminator parameters, said illumination source transmitting light energy through a mask having a pattern corresponding to the layout, said mask having selected mask parameters, the exposing being limited by a selected numerical aperture (NA); wherein the selected illuminator parameters, mask parameters and NA correspond to one of the selected RETs" as recited in claim 12. The Examiner cites paragraphs [0003]; [0049] and [0050] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 6. Applicants respectfully traverse. As stated above, Maurer instead discloses that the basic resolution of an optical lithography system is generated related to a ratio of Lambda/NA of an optical wavelength of the radiation used for exposure to the numerical aperture of the optical system used to direct radiation from an irradiated mask to the wafer. [0003]. Maurer further discloses that other RETs such as double-

exposure dipole lithography (DDL) use off-axis mask illumination. [0049]. Maurer further discloses that the DDL and other off-axis illumination RETs are generally optimized for a particular pitch, typically a rather dense pitch. [0050]. There is no language in the cited passages that discloses that the selected illuminated parameters, mask parameters and NA correspond to one of the selected RETs. Thus, Maurer does not disclose all of the limitations of claim 12, and thus Maurer does not anticipate claim 12. M.P.E.P. §2131.

Applicants further assert that Maurer does no disclose "wherein simulating how structures within the layout will pattern for a plurality of RETs is performed using the same simulation engine as is used to perform OPC on the layout" as recited in claim 15. The Examiner cites paragraphs [0072-0074] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 6. Applicants respectfully traverse and assert that Maurer instead discloses that the hierarchical database 702 is configured for access by layout verification tools such as a layout versus schematic (LVS) tool 708, a design rule check (DRC) tool 710, an optical rule checking (ORC) tool 712, a phase-shift mask (PSM) tool 714, and an optical process correction (OPC) tool 716 that are configured to verify that transformation to a physical layout has not introduced errors, and that the final layout is in compliance with appropriate geometric design rules or other design rules. [0072]. Maurer further discloses that the tool 700 also includes a data export component 718 configured to provide data to a circuit manufacturing process 720. [0073]. Maurer additionally discloses that the tool 700 can be implemented using a work-station, personal computer, one or more network computers, or other computer systems. [0074]. There is no language in the cited passages that discloses simulating how structures within the layout will pattern for a plurality of RETs is performed using the same simulation engine as is used to perform OPC on the layout. Thus, Maurer does not disclose all of the limitations of claim 15, and thus Maurer does not anticipate claim 15. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "wherein the simulating step is automated with respect to performing OPC on the layout" as recited

in claim 15. The Examiner cites paragraphs [0072-0074] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 6. Applicants respectfully traverse. As stated above, Maurer instead discloses that the hierarchical database 702 is configured for access by layout verification tools such as a layout versus schematic (LVS) tool 708, a design rule check (DRC) tool 710, an optical rule checking (ORC) tool 712, a phase-shift mask (PSM) tool 714, and an optical process correction (OPC) tool 716 that are configured to verify that transformation to a physical layout has not introduced errors, and that the final layout is in compliance with appropriate geometric design rules or other design rules. [0072]. Maurer further discloses that the tool 700 also includes a data export component 718 configured to provide data to a circuit manufacturing process 720. [0073]. Maurer additionally discloses that the tool 700 can be implemented using a work-station, personal computer, one or more network computers, or other computer systems. [0074]. There is no language in the cited passages that discloses that the simulating step is automated with respect to performing OPC on the layout. Thus, Maurer does not disclose all of the limitations of claim 16, and thus Maurer does not anticipate claim 16. M.P.E.P. §2131.

Applicants further assert that Maurer does not disclose "wherein the simulating step is performed automatically using the same simulation engine as is used for performing optical proximity correction (OPC) and mask data preparation" as recited in claim 21. The Examiner cites paragraphs [0072-0074] of Maurer as disclosing the above-cited claim limitation. Office Action (6/13/2006), page 6. Applicants respectfully traverse. As stated above, Maurer instead discloses that the hierarchical database 702 is configured for access by layout verification tools such as a layout versus schematic (LVS) tool 708, a design rule check (DRC) tool 710, an optical rule checking (ORC) tool 712, a phase-shift mask (PSM) tool 714, and an optical process correction (OPC) tool 716 that are configured to verify that transformation to a physical layout has not introduced errors, and that the final layout is in compliance with appropriate geometric design rules or other design rules. [0072]. Maurer further discloses that the tool 700 also includes a data export component 718 configured to provide data to a circuit manufacturing process 720.

[0073]. Maurer additionally discloses that the tool 700 can be implemented using a work-station, personal computer, one or more network computers, or other computer systems. [0074]. There is no language in the cited passages that discloses that the simulating step is performed automatically using the same simulation engine as is used for performing optical proximity correction (OPC) and mask data preparation. Thus, Maurer does not disclose all of the limitations of claim 21, and thus Maurer does not anticipate claim 21. M.P.E.P. §2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Maurer, and thus claims 1-24 are not anticipated by Maurer. M.P.E.P. §2131.

III. CONCLUSION:

As a result of the foregoing, it is asserted by Applicants that claims 1-24 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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